REMARKS

The Applicants request reconsideration of the rejection.

Claims 12-31 are pending.

Claims 12-14, and 21-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardenfors et al, U.S. 6,477,148 (Gardenfors), in view of Brett, U.S. 6,400,541 (Brett), and Bando et al., U.S. 6,700,792 (Bando). Claims 15, 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardenfors in view of Brett, Bando, and Lu, U.S. 4,989,057 (Lu). The Applicants traverse as follows.

Gardenfors is cited as disclosing the basic structure of a communication semiconductor integrated circuit device, including a transmission unit, a reception unit, and a terminal. As noted in the Office Action, Gardenfors does not disclose a protection circuit coupled to a low noise amplifier transistor as claimed in Claim 12. Thus, the Examiner cites Brett as disclosing this feature.

Specifically, the Examiner cites Brett as disclosing a protection device comprising a protection unit 20 coupled to a

low noise amplifier 10, a first voltage line Vcc, and a second voltage line Vee, wherein the protection circuit includes a first protection circuit 50 and a second protection circuit 52 which are coupled between the first voltage line and the second voltage line.

Respectfully, however, these findings in Brett do not meet the limitations of Claim 12. More particularly, Claim 12 recites a protection unit formed on a semiconductor chip and coupled to a low noise amplifier transistor, to a first voltage line arranged to be supplied with a first voltage having a first potential, to a second voltage line arranged to be supplied with a second voltage having a second potential that is different from the first potential, and to a terminal formed on the semiconductor chip and coupled to the low noise amplifier transistor. Claim 12 further requires that the protection unit include a first protection circuit coupled between the first voltage line and the terminal and which allows an electric current to flow from the first voltage line to the terminal at a protection time against an electrostatic breakdown, and a second

protection circuit coupled between the second voltage line and the terminal and which allows an electric current to flow from the terminal to the second voltage line at a protection time against an electrostatic breakdown, the first and second protection circuits being directly electrically connected in common to the terminal.

Referring to Brett, the patent discloses a protection circuit 20 connected to differential inputs IP and IPB of a low noise amplifier 10. The protection circuit 20 is also connected to supply lines Vcc and Vee, as indicated in the Office Action.

The protection circuit 20 includes diode 50 (the "first protection circuit" cited in the Office Action) and diode 52 (the "second protection circuit" cited in the Office Action). Diode 50 is forward-biased between virtual ground node 36 and supply line Vcc, and diode 52 is forward-biased between supply line Vee and virtual ground node 36. According to the patent, diodes 50 and 52 should have a reverse breakdown voltage which is as small as possible, while still exceeding the maximum

required supply voltage of the circuit by a reasonable safety margin.

Discharge paths for all possible electrostatic discharge (ESD) events involving input pin IP are shown in Table 1, Column 4 of the patent. By symmetry, similar paths exist for all ESD events involving input pin IPB.

Table 1 shows a discharge path between input path IP and supply line Vee via forward-biased diode 30 and reverse-biased diode 52. Another discharge path is between supply line Vee and input IP via forward-biased diode 52 and forward-biased diode 32. Like forward- and reverse-biased discharge paths via diode 50 exist between input pin IP and supply line Vcc.

Thus, the person of ordinary skill in the art readily sees that the amended Claim 12 clarifies a patentable distinction between Claim 12 and the combination including Brett. Note that the common node directly electrically connecting diode 50 and diode 52 of Brett is virtual ground node 36, and not the terminal as required by Claim 12. Thus, the combination including Brett fails to render obvious the claimed invention.

Regarding the dependent claims, numerous separately patentable features are recited. However, the Office Action does not address the dependent claims with specificity. The Applicants draw the Examiner's attention particularly to Claim 14, which requires that an output of the low noise amplifier transistor be supplied to the terminal; however, the Office Action asserts the motivation to combine Gardenfors with Brett by referring to the desire "to protect the input of LNA and the power supplies for ESD event."

Regarding the rejection of dependent Claims 15 and 17-20, this rejection relies upon an additional secondary reference to Lu. In particular, the Office Action states that the Lu reference discloses that the ESD protection comprising a plurality of protection circuits which are coupled between the first power line and the second power line are MOSFET transistors.

Notably, the Lu reference relates to electrostatic discharge protection circuit for semiconductor-on-insulator circuits.

In SOI circuits, as opposed to circuits on a traditional bulk semiconductor substrate, all the electrostatic energy is dissipated to the thin semiconductor layer because most electrically-insulative materials are poor thermal conductors. The heat energy becomes excessive, which poses the danger of destruction to the integrated circuit. Consequently, Lu provides a plurality of protection circuits for a low voltage drop thereacross to thereby reduce the thermal energy dissipation requirements of the thin semiconductor layer on the SOI structure.

Further, the direction of the electric current at a protection time against an electrostatic breakdown in the Lu reference is different from the present invention as claimed in the rejected claims.

Referring to Claim 15, a third protection circuit is coupled between the first voltage line and the terminal and which allows an electric current to flow from the terminal to the first voltage line at a protection time against an electrostatic breakdown, and a fourth protection circuit is

coupled between the second voltage line and the terminal and which allows an electric current to flow from the second voltage line to the terminal at a protection time against an electrostatic breakdown. By this construction, the third and fourth protection circuits protect the internal circuit against positive/negative electrostatic discharge by combining the first and the second protection circuits (which have a different current flow at a protection time against an electrostatic breakdown) with the third and fourth protection circuits.

Thus, each of Claims 15 and 17-20 is patentably distinguishable from the combination of Gardenfors, Brett, Bando and Lu.

In closing, the Applicants note that Claim 16 is not rejected on prior art grounds. Claim 16 is similar to claims 21 through 23 in that the second potential on the second voltage line is lower than the first potential on the first voltage line. Claims 21-23 were rejected over the combination of Gardenfors, Brett, and Bando, but the rejection does not address this limitation (the rejection also does not address the

limitation of Claims 24-26, in which it is required that the first potential be lower than the second potential). The Applicants assert all rights in the subject matter of these and all of the pending claims.

In view of the foregoing amendments and remarks, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,

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